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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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09/593,945

06/15/2000

Hitoshi Naoe

1247-0428P-SP

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7590

11/30/2004

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EXAMINER

MUNOZ, GUILLERMO

ART UNIT

PAPER NUMBER

2637

DATE MAILED: 11/30/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/593,945

Applicant(s)

NAOE, HITOSHI

Examiner

Guillermo Munoz

Art Unit

2637

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 09 August 2004.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-15 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☒ Claim(s) 3,4,6,7,9 and 12 is/are allowed.
- 6) ☒ Claim(s) 1,2,5,8,10,11 and 13-15 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☒ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☐ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date _____
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____

DETAILED ACTION

Response to Arguments

Applicant's arguments on pages 8-9 of amendment filed August 9, 2004, regarding claim 1, have been fully considered but they are not persuasive.

Applicant's argument—

Applicant argues Tajima's phase comparison circuit performs phase comparisons of input data and poly phase clocks, while Applicants invention detects phase shift of the clock by comparing an input clock signal to delayed clock signals.

Examiner's response—

Examiner refers applicant to instant application page 1, Description of the Related Art, wherein Applicant disclose well known and generally understood methods of combining timing information and data for transmission over one line "in many cases, high speed serial communication does not use a separate line for the timing information from the line for the data" lines 17-19. The input data signal having timing information is interpreted as the input clock signal.

Furthermore, In response to applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e., comparing an input clock signal to a delayed clock signals) are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

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Applicant's arguments on pages 9 of amendment filed August 9, 2004, regarding claim 5, have been fully considered but they are not persuasive.

Applicant's argument—

Applicant argues Tajima's holding circuit "holds an output phase for clock determination during a period receiving one frame of input data" in page 9, line 17, while Applicants invention samples an output from the detection circuit a plurality of times and carries out operations on sampled values.

Examiner's response—

Examiner refers applicant to instant application, wherein the operation of the operational circuit is defined as "a mean value of the sampled outputs" on page 22, line 7-8. Additionally, Instant Application exemplifies an output from the detection circuit as being "0000001111110", note page 28, line 19.

Using the broadest reasonable interpretation consistent with the specification examiner interprets the function of the operational circuit to be providing center position by averaging a plurality of outputs from the detection circuit, which is equivalent to the operation of the determining circuit, see Tajima et al. Col. 3, lines 1-3. The operation carried out on the average of the Tajima et al.'s determining means is to hold it for a period of time by the holding circuit.

Applicant's arguments on pages 10 of amendment filed August 9, 2004, regarding claim 8, have been fully considered but they are not persuasive.

Applicant's argument—

Applicant argues Tajima's flip-flops are not "bit synchronous working circuits", note lines 3-13.

Examiner's response—

The "bit synchronous working circuits are interpreted as a type of digital circuit configured to perform a predetermined operation on a signal synchronously. The reference teaches decision circuit 4 performing such a predetermined operation on a data signal synchronously; therefore, it is a synchronous circuit.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in a patent granted, on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) do not apply to the examination of this application as the application being examined was not (1) filed on or after November 29, 2000, or (2) voluntarily published under 35 U.S.C. 122(b). Therefore, this application is examined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

Claims 1-2, 5, 8, 10, 11, 13, 14 and 15 are rejected under 35 U.S.C. 102(e) as being anticipated by Tajima et al. (cited in Office Action mailed May 7, 2004).

Regarding claim 1, Tajima et al. discloses a Bit Synchronization Circuit, which teach all the claimed subject matter “a polyphase clock generation circuit...detection result from the detection circuit” in claim 1 as follows. Tajima et al. disclose that a bit synchronization circuit comprises a multi-phase clock generating means, a phase comparator means for comparing between the input data and respective clocks of different phases output from the multi-phase clock, a phase determining means for determining the clock occurring substantially at the data bit center and selection means for taking the clock determined by the phase determining means as the data decision clock, note Col. 2, line 53 – Col. 3, line 10.

Regarding claim 2, Tajima et al. further teach the claimed subject matter, note figure 2 and Col. 3, lines 51-52.

Regarding claim 5; as applied to claim 1 above, Tajima et al. further teach the claimed subject matter “operational circuit....carrying out operations on sampled values” in lines 10-12 as follows. Tajima et al. disclose a holding circuit (element 8, of figure 8) used to hold the phase for decision of data during receiving of one frame of data, note figure 8 and Col. 6, lines 57-60.

Regarding claim 8; as applied to claim 1 above, Tajima et al. further teach the claimed subject matter “a plurality of bit synchronous working circuits...carried out at each different phase” in claim 8, lines 10-16 as follows. Tajima et al. teach a plurality of decision means (element 4 of figure 1) used to generate data decisions using different phases output from the multi-phase clock, note figure 1 and Col. 2, lines 59-61.

Regarding claim 10, Tajima et al. further teach the claimed subject matter "constant cycle time" as follows. Tajima et al. disclose holding the detection circuit output for the period of time required to receive a data frame, note Col. 6, lines 57-60.

Regarding claim 11, see claim 1.

Regarding claim 13, see claim 2.

Regarding claim 14, see claim 2.

Allowable Subject Matter

Claims 3, 4, 6, 7, 9 and 12 are allowed for reasons described in Office Action mailed May 7, 2004.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

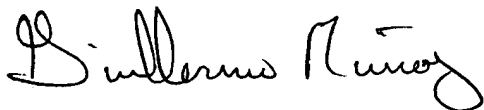
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Any inquiry concerning this communication or earlier communications from the examiner should be directed to Guillermo Munoz whose telephone number is 571-272-3045.

The examiner can normally be reached on Monday-Friday 8:30a.m-4:30p.m..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jay Patel can be reached on 571-272-2988. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



GM
November 24, 2004



JEAN B. CORRIEUS
PRIMARY EXAMINER

11-24-04